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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/469,409	12/22/1999	BRIAN A. PETERSEN	M-7907-US	4940

33031 7590 01/28/2003

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EXAMINER

POLLACK, MELVIN H

ART UNIT	PAPER NUMBER
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2142

DATE MAILED: 01/28/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/469,409

Applicant(s)

PETERSEN ET AL.

Examiner

Melvin H Pollack

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 13 November 2002.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: *see attached office action*.

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments filed November 13, 2002, have been fully considered but they are not persuasive. The reasons are listed below.

2. Applicant defines "parsing a packet...to determine a vector" in Page 5, lines 1-8. "Packet parser 120 takes a quick look at the received packet and assigns a 'vector' to the packet that indicates to central processor 110 in which of several categories (based on, e.g., packet formats) the packet belongs. A vector, as used here, is an identifying number or data field... Knowing the packet vector, central processor 110 knows where in the packet the fields of interest are located without having to examine the packet itself." In other words, the packet is looked at, and then assigned a category field that is reviewed by another component. It does not have to be stored anywhere, especially as drawn in the claims. This is consistent with the definitions drawn in the art. If the applicant wishes more functionality, then an amending of the independent claims is required.

3. Applicant charges that Examiner has not shown prima facie evidence to "parsing a packet...to determine a vector." Examiner will make it clearer here. The quoted portion is that a copy of the packet header is "forwarded... to the search engine 315, which searches the database 320 to determine... if there is information... such as the type of packet." This idea is also shown in the abstract, lines 6-7 and in other parts of the specification (e.g., col. 1, line 65 – col. 2, line 2). In this teaching, the search engine 315 acts as a packet parser, because it looks at the header, and then uses the database to determine category information. This category information is then

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used to determine how to process the packet, just as in the applicant's invention (col. 6, lines 10-12, flesh out this last point in greater detail).

4. Applicant added emphasis to the phrase "if there is" in order to presumably question this aspect. Examiner clarifies by responding that not every packet that passes through the system has to be parsed, or requires a header update, and the system is set up to handle these eventualities (col. 6, lines 19-22). More information can be shown in Fig. 3-6, with special emphasis on Fig. 5, #515-520.

5. Applicant's other argument is that Muller fails to show that the one or more peripheral processors "comprise a register set." Applicant teaches that the peripheral processors (Fig. 1, #120-150 and Page 4, lines 3-11) are the items that handle the methods of claim 1. Applicant also states that "Any implementation form may be selected... the present invention is not limited in the physical implementation of any PP." The examiner notes that nowhere in the specification does it teach an implementation of the peripheral processors in any configuration that comprises a register set, and Fig. 1 seems to show that the PP are not. Page 7, lines 19-25, shows that they "share a common set of registers." The examiner thus interprets this limitation to mean that each processor has a register set, as any other interpretation would require the amending of claim 6 and/or the addition of new subject matter.

6. Examiner begins by explaining the structure of Muller. In Muller, a central processing module (Fig. 1, #160) talks to a set of subsystems (Fig. 1, #110) that includes a switch element (Fig. 1, #111), which then consists of a set of components (Fig. 2). The process of the CPU controlling said items is shown in col. 4, lines 20-34. One of these items, Fig. 2, #210, consists of the items in Fig. 3, which are the peripheral processors as defined by the application, and thus

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are shown to have a direct communication of the CPU (col. 4, line 55 – col. 5, line 14). And the peripheral processors share a common set of registers (Fig. 3, #310, 325, 327) as does each grouping of peripheral processor (Fig. 2, #230). The fact that they are not specifically called registers does not matter as long as they perform the duties of the register, as shown (col. 6, lines 60-65). Further, applicant has failed to show the importance of the register, and in fact taught away from this aspect by writing very little regarding the register set (such as its purpose) and by teaching that a multitude of hardware configurations will do. And the record of art clearly shows that registers are well known in the art, and easily added to the hardware components.

7. For the above reasons, a case of prima facie anticipation has been shown. Therefore, the applicant's arguments are non-persuasive.

8. Examiner notes that applicant has not addressed the items of art added to reject the dependent claims.

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

10. Claims 1-3, 6, 7, 13-17, 20-22, and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Muller et al. (6,128,666).

11. For claim 1, Muller teaches a method (see abstract) of packet processing (col. 1, lines 10-15) comprising:

- a. Parsing a packet, said packet having a header portion, to determine a vector (Fig. 3, #310-320, and all proof listed above);
  - b. Coordinating processing using said vector (Fig. 5, #515-520, Fig. 7);
  - c. Deconstructing said packet header to form header data (col. 6, lines 5-10, where it is anticipated that the extraction of header data from the header is a required first step to analysis of the aforementioned header data.);
  - d. Searching one or more data structures based on said header data to produce search results (col. 6, lines 26-32);
  - e. Editing said packet based on said search results, said header data, and said vector (Fig. 3, #330);
  - f. Said coordinating further comprises monitoring said deconstructing, said searching, and said editing (col. 3, lines 62-65).
12. As for claim 2, Muller teaches that said coordinating further comprises sharing data with said parsing, said deconstructing, said searching, and said editing (Fig. 3).
13. As for claim 3, Muller teaches that said packet is buffered before said parsing (col. 6, lines 1-2).
14. For claim 6, Muller teaches an apparatus (see abstract and above proof) for packet processing, comprising:
  - a. A central processor for packet processing, said central processor comprising a register set (col. 3, lines 55-62); and

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- b. One or more peripheral processors each connected to said central processor and each comprising a register set (col. 3, lines 56-58), wherein each said peripheral processor returns at least one datum to said central processor (Fig. 2); wherein
- c. Said central processor communicates with said peripheral processor (col. 3, lines 62-65).

15. As for claim 7, Muller teaches that the central processor comprises a general purpose processor (col. 3, line 59, and col. 10, lines 28-32. It is anticipated that the processor can participate in a variety of functions, making it a general purpose processor.).

16. As for claim 13, Muller teaches that a portion of each said peripheral register set is mapped onto said central processor register set (col. 3, lines 60-62).

17. As for claim 14, Muller teaches that said central processor and at least one peripheral processor together form at least a part of a single application specific integrated circuit (col. 4, lines 20-34).

18. Claims 15-17 are drawn to a computer system for packet processing, comprising computer instructions for implementing the method drawn in claims 1-3, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Therefore, if claims 1-3 are rejected, then claims 15-17 are also rejected for the reasons above.

19. Claims 20-22 are drawn to a computer-readable storage medium, comprising computer instructions for implementing the method drawn in claims 1-3, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method.

Official notice is also taken that computer instructions would be stored on a computer-readable

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medium such as a disk or memory. Therefore, if claims 1-3 are rejected, then claims 20-22 are also rejected for the reasons above.

20. Claims 25-27 are drawn to a computer data signal embodied in a carrier wave, comprising computer instructions for implementing the method drawn in claims 1-3, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Therefore, if claims 1-3 are rejected, then claims 25-27 are also rejected for the reasons above.

***Claim Rejections - 35 USC § 103***

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

22. Claims 1-7, 13-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller as applied to claims 1-3, 6, 7, 13-17, 20-22, and 25-27 above, and further in view of Turner et al. (6,018,524).

23. For claims 1-3, 6, 7, 13-17, 20-22, and 25-27, that which is anticipated is obvious.

24. As for claim 4, Muller does not go into detail regarding the nature of the search method, treating it as a black box. Turner, which goes into significant detail regarding search methods in the process of packet analysis and routing, teaches that said deconstructing further comprises forming a search argument, and said searching uses said search argument (col. 7, lines 25-34). Further, this step would be obvious under Muller, due to the claim 1 discussion above, since the extraction of data for search purposes would automatically make said data a "search argument"

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by definition. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use Turner's router search method in Muller's router search black box as a way of implementing that particular feature.

25. Claim 5 has many of the same limitations as claim 4. However, the method further consists of said coordinating further comprises operating on said search argument to form a modified search argument prior to said searching, and said searching uses said modified search argument. Turner also teaches the modification of a search argument (col. 11, lines 15-18). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use Turner's router search method in Muller's router search black box as a way of implementing that particular feature.

26. Claims 18 and 19 are drawn to a computer system for packet processing, comprising computer instructions for implementing the method drawn in claims 4 and 5, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Therefore, if claims 4 and 5 are rejected, then claims 18 and 19 are also rejected for the reasons above.

27. Claims 23 and 24 are drawn to a computer-readable storage medium, comprising computer instructions for implementing the method drawn in claims 4 and 5, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Official notice is also taken that computer instructions would be stored on a computer-readable medium such as a disk or memory. Therefore, if claims 4 and 5 are rejected, then claims 23 and 24 are also rejected for the reasons above.

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28. Claims 28 and 29 are drawn to a computer data signal embodied in a carrier wave, comprising computer instructions for implementing the method drawn in claims 4 and 5, respectively. It is considered in the prior art that a system implementation is logically equivalent to the underlying method. Therefore, if claims 4 and 5 are rejected, then claims 28 and 29 are also rejected for the reasons above.

29. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller as applied to claim 6 above, and further in view of VanDervort et al. (5,761,191).

30. For claim 8, VanDervort teaches that the central processor comprises a microsequencer (col. 7, lines 7-9). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of ordinary skill in the art would have used a microsequencer CPU in Muller's invention to fulfill the necessary implementation aspects.

31. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller as applied to claim 6 above, and further in view of Vahalia et al. (6,275,953).

32. For claim 9, Vahalia teaches that the central processor comprises more than one processor acting in concert (col. 2, lines 6-9). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of ordinary skill in the art would have used a parallel processor CPU in Muller's invention to fulfill

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the necessary implementation aspects and to make the invention more flexible and less prone to error.

33. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller as applied to claim 6 above, and further in view of Eames et al. (6,078,593).

34. For claim 10, Eames teaches that one or more of said peripheral processors comprise fixed logic circuits (col. 21, lines 1-5). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of ordinary skill in the art would have used a fixed logic peripheral processor in Muller's invention to fulfill the necessary implementation aspects.

35. As for claim 11, Eames teaches that one or more of said peripheral processors comprise programmable logic circuits (col. 21, lines 1-5). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of ordinary skill in the art would have used a programmable logic peripheral processor in Muller's invention to fulfill the necessary implementation aspects.

36. As for claim 12, Eames teaches that one or more of said peripheral processors comprise a programmable state machine (col. 21, lines 44-48). Muller does not discuss the particular implementation of either the central processor or the peripheral processors, so the choice is necessary in order to complete the implementation. At the time the invention was made, one of

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ordinary skill in the art would have used a programmable state machine peripheral processor in Muller's invention to fulfill the necessary implementation aspects.

***Conclusion***

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin H Pollack whose telephone number is (703) 305-4641. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark R Powell can be reached on (703) 305 - 9703. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

A handwritten signature in black ink, appearing to read 'R. B. Harrell', with a large, stylized loop at the beginning and a horizontal line extending to the right.

MHP

January 24, 2003

**ROBERT B. HARRELL  
PRIMARY EXAMINER**